Please amend Claims 1-5, 8-19, 21 as indicated below while also canceling Claim 20, and adding new Claims 22-67 as shown.

-- 1. (Amended once) A field programmable gate array (FPGA) device [*100,1000*] comprising:

(a) a first plurality, P1 of repeated logic units [*VGBs,102,1021*] wherein:

(a.1) each said logic unit is user-configurable to acquire and process at least a second plurality, P2 of input logic bits [*Fig.6A*] and to responsively produce result data having at least a third plurality, P3 of output logic bits [*Fig.6B*],

(a.2) said logic units are distributed among a plurality of horizontal rows, with each row of the plurality of rows having a fourth plurality, P4 of said logic units;

(b) a fifth plurality, P5 of horizontal interconnect channels (HIC's) [*150*] correspondingly distributed adjacent to said horizontal rows of logic units, wherein:

(b.1) each said horizontal interconnect channel (HIC) includes at least P3 interconnect lines, and

(b.2) each said horizontal row of P4 logic units is configurably couplable to at least a corresponding one of the [P6] P5 HIC's at least for acquiring input logic bits from the corresponding HIC [or at least] and for outputting result data to the corresponding HIC;

(a.3) wherein each of said logic unit can internally process its respective second plurality of input logic bits without using said horizontal interconnect channels or other general interconnect for such internal processing; and

(c) an embedded memory subsystem [*114/116*], wherein said embedded memory subsystem includes:

(c.1) a sixth plurality, P6 of independently-useable memory blocks [ML0-MR7], and wherein:

(c.1a) each said independently-useable memory block is embedded within one of said rows of logic units [*102*] and is configurably couplable to the corresponding HIC of said row for transferring storage data by way of the corresponding HIC of that row of P4 logic units; and

(c.1b) each of said memory blocks includes at least a first address-capturing register [*1011*] that is programmably couplable [*1062,1064*] to at least one of said HIC's [*1050*] for receiving and capturing in synchronism with a supplied address-strobing signal [*ADRCLK*] , an address signal [*1051,1052*] supplied on said at least one HIC;

(c.1c) each of said memory blocks includes at least a first data-capturing register [*10R2*] for capturing said storage data [*Din,Dout*] in synchronism with a supplied first data-strobing signal [*RWCLK1*] ; and

(c.1d) each first address-capturing register is clockable by a first address-strobing signal [*1015*] that is independent of the first data-strobing signal.--

2. (Amended once) A FPGA device [*100*] according to Claim 1 wherein:

(a.3) said logic units are further distributed among a plurality of vertical columns, with each column of the plurality of columns having a seventh plurality, P7 of said logic units; and

(c.1b1) plural ones of said memory blocks are arranged to define one or more columns [*114/116*] of embedded memory within said FPGA device [*100*] with each such column having an eighth plurality, P8 of said memory blocks.--

A 3. (Amended once) A field programmable gate array device [*100*] according to Claim 2 wherein:

(c.1c1) each said memory block is organized as a ninth plurality, P9 of addressable sets of storage data bits, where each addressable set of storage data bits includes at least P3 bits that are transferable by way of the corresponding HIC of its corresponding row of P4 logic units, said P3 plurality of bits [number] corresponding to the P3 plurality [number] of output logic bits producible by each said logic unit.--

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B 4. (Amended once) A field programmable gate array device [*100*] according to Claim 3 wherein:

(c.1c2 [1]) each of P2 and P3 is an integer equal to or greater than 4.--

C 5. (Amended once) A field programmable gate array device [*100*] according to Claim 1 wherein:

(a.3) groups of said logic units are further wedged together such that no HIC's pass between the wedged together logic units, and such that each group of logic units defines a logic superstructure [*101,440*]; and

(c.1c2) groups of said memory blocks [*470,480*] are also wedged together such that no HIC's pass between the wedged together memory blocks, and such that each group of memory blocks defines a memory superstructure that is configurably-couplable to a corresponding logic superstructure [*440*].

6. A field programmable gate array device [*100*] according to Claim 1 wherein said embedded memory subsystem includes:

(c.2) at least one special interconnect channel [*466*] for supplying address signals to the first address-capturing registers [*1011*] of a respective set of said memory blocks.

7. A field programmable gate array device [*100*] according to Claim 6 wherein:

(c.1b1) there are at least two of said columns [*114/116*] of embedded memory; and

(c.2a) there are at least two of said special interconnect channels [*164,166*], and each respective special interconnect channel is for supplying address signals to a respective one of the at least two columns of embedded memory.

-- 8. (Amended once) A field programmable gate array device [*100*] according to Claim 6 wherein:

(c.1c3) each said memory block has at least first and second data ports [*884,882*] each for outputting storage data;

(c.1d) each said memory block has at least first and second address ports [*874,872*] each for receiving address signals identifying the storage data to be output by a corresponding one of the at least first and second data ports;

(c.1e) each said memory block has in addition to said respective first address-capturing register, a second address-capturing register [*1012*] that is programmably couplable [*1062,106C*] to at least one of said HIC's [*1050*] for receiving and capturing an address signal [*1051,1052*] supplied on said at

least one HIC, and said first and second address-capturing registers respectively service the first and second address ports; and

(c.2a) the at least one special interconnect channel includes first and second address-carrying components [*862a,862b*] along which independent address signals may be respectively carried for application to respective ones of the first and second address ports [*874,872*] of at least two memory blocks.--

9. (Amended once) A field programmable gate array device [*100*] according to Claim [1] 6 wherein:

(c.1d) each said memory block has a controls-receiving port [*873*] for programmably acquiring from said at least one special interconnect channel, control signals that control operations of said memory block; and

(c.1e) [each respective first address-capturing register is clocked by a respective first address clock signal] said first address-strobing signal [*ADRCLK1,1015*] is acquired by said controls-receiving port.--

10. (Amended once) In a field programmable gate array device (FPGA) [*100*] having a user-configurable interconnect network that includes a plurality of horizontal interconnect channels [*150*] each with a diversified set of long-haul interconnect lines [*MaxL*] and shorter-haul interconnect lines [*2xL-8xL*], an embedded memory subsystem [*114/116*] comprising:

(a) a plurality of multi-ported memory blocks [*ML0-MR7*] each arranged adjacent to a horizontal interconnect channel (HIC) [*850*] of the interconnect network;

wherein:

(a.1) each multi-ported memory block [*870*] includes a first, independently-addressable data port [*884*] and a second, independently-addressable data port [*882*];

(a.2) each of said first and second, independently-addressable data ports includes a respective address-capturing register [*1011,1012*] that is connectable by user-configurable intercouplings [*855*] to one or both of the long-haul interconnect lines [*859*] and the shorter-haul interconnect lines [*852-858*] for capturing a respective address signal [*1051,1052*] in synchronism with a supplied, address-strobing signal [*1015*]; and

(a.3) each of said first and second, independently-addressable data ports includes a respective, read data-capturing register [*10R2,10R3*] that is connectable by user-configurable intercouplings [*1075,10B2,10B3*] to at least the long-haul interconnect lines [*10A2*] for capturing respective read data of the port independently of the address-strobing signal and for outputting the captured read data to the long-haul interconnect lines.--

14 11. (Amended once) In an FPGA device having a plurality of variable grain, configurable logic blocks (VGB's) [*102*] and VGB interconnect resources including lines of diversified continuous lengths [*2xL-8xL,MaxL*] for interconnecting said VGB's, an embedded memory subsystem comprising:

a special interconnect channel [*1060*], programmably couplable to said VGB interconnect resources; and

a plurality of memory blocks [*470,480*] wherein each memory block includes:

(a) at least a first address-capturing register [*1011*] that is programmably couplable [*1062,1064*] to said VGB interconnect resources [*1050*] by way of said special interconnect

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channel for receiving and capturing a respective first address signal [*1051,1052*] supplied by way of said VGB interconnect resources and said special interconnect channel; and

(a.1) address-strobing means [*1055,1065*] for strobing the first address-capturing register by way of said VGB interconnect resources and said special interconnect channel, where said address-strobing can occur independently of data-capture strobing for corresponding data.--

12. (Amended once) The embedded memory subsystem of Claim 11 wherein each memory block further includes:

(b) a second address-capturing register [*1012*] that is programmably couplable [*1062,1064*] to said interconnect resources [*1050*] for receiving and capturing a respective second address signal [*1051,1052*] supplied by way of said VGB interconnect resources.--

13. (Amended once) The embedded memory subsystem of Claim 11 wherein:

(a.1) said first address-capturing register [*1011*] is further programmably couplable [*1065*] to said VGB interconnect resources [*1057*] by way the special interconnect channel for receiving a respective first address clock signal [*ADRCLK1,1015*] to which the first address-capturing register is responsive.--

14. (Amended once) A method [*Fig.10*] for use in an FPGA device having plural variable grain blocks (VGB's) [*102*], [diversified] configurable interconnect resources with continuous conductors of diversified lengths, and an embedded memory subsystem comprising a plurality of memory blocks [*870*] situated for configurable coupling to the diversified interconnect resources, where the memory blocks each have at least one

address input port [*872,874*] and at least one data port [*882,884*], the address input port having a respective address-capturing register [*1011*], said method comprising the steps of:

(a) outputting [*1023,1031*] a first address signal for conveyance by at least part of said interconnect resources [*1051,1052*] to a respective first address-capturing register of an address input port of a given memory block;

(b) outputting [*1055*] a first address-strobing signal [*1057*] for conveyance by at least part of said interconnect resources to the respective first address-capturing register to thereby capture [capturing] the conveyed first address signal in the respective first address-capturing register [*1011*] of the given memory block; and

(d) coupling the first address-strobing signal through delaying logic [*1021,1022*] for thereby invoking a delay in [while the first address signal is captured,] outputting [*1027,1032*] of a next address signal for conveyance by at least part of said interconnect resources to the respective first address-capturing register of the address input port of the given memory block, said invoked delay assuring that the first address signal is captured by the respective first address-capturing register before the outputting of said next address signal.--

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A 15. (Amended once) The method of Claim 14 wherein at least one of said step (a) of outputting the first address signal and said step (d) of coupling the first address-strobing signal through delaying logic includes the substep of:

(a/d.1) transmitting the first address signal through a configurable sequential output element [*CSEQ,1023*] of a first of said VGB's.--

A 16. (Amended once) The method of Claim 15 wherein at least one of

said step (a) of outputting the first address signal and said step (d) of coupling the first address-strobing signal through delaying logic includes the further substep of:

(a/d.2) sourcing the first address signal from a storage register [*1022*] within a configurable sequential element [*CSE*] of said first of said VGB's.--

17. (Amended once) The method of Claim 16 wherein at least one of said step (a) of outputting the first address signal and said step (d) of coupling the first address-strobing signal through delaying logic includes the further substep of:

(a/d.3) applying an address-changing clock signal [*1022a*] to the storage register that sources the first address signal, where said address-changing clock signal is derived from [an address-validating clock] the first address-strobing signal [*1057*] .

[applied to the address-capturing register.] --

18. (Amended once) The method of Claim 14 wherein said step (a) of outputting the first address signal includes the substeps of:

(a.1) transmitting the first address signal through a first of plural tristate drivers [*1031,1032*], where each of the tristate drivers has an output enabling terminal [*1035,1036*];

(a.2) providing an address-changing control signal [*1043*] that deactivates the output enabling terminal [*1035*] of the first tristate driver, where said address-changing control signal is derived from [an address-validating clock] the first address-strobing signal [*1057*]

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[applied to the address-capturing register.] --

19. (Amended once) A method [*Fig. 10*] for configuring an FPGA device having plural variable grain blocks (VGB's) [*102*], configurable interconnect resources, and an

embedded memory subsystem comprising one or more memory blocks [*870*] situated for configurable coupling via the configurable interconnect resources to the VGB's, where the memory blocks each have at least one registered address input port [*872*] for receiving and storing supplied address bits, and where the memory blocks each further have at least one registered data output port [*882*] for storing and outputting retrieved read-data, said method comprising the steps of:

(a) defining a first route [*1025,1062,1064*] through said interconnect resources from an address signal sourcing circuit [*1023,1031*] of the FPGA device to the at least one registered address input port [*872*]; [and]

(b) defining a second route [*1057,1067,1065*] through said interconnect resources from an address clock sourcing circuit [*1055*] of the FPGA device to the at least one registered address input port;

(c) defining a third route [*1001*] through said interconnect resources from the address clock sourcing circuit [*1055*] to an address-changing circuit [*1021,1040*] of the FPGA device, the third route being configured such that a new address signal can be produced by action of said address-changing circuit substantially at the same time or shortly after an address clock signal [*1015*] of the address clock sourcing circuit [*1055*] clocks the at least one registered address input port, said new address signal being produced so as to not interfere with a current address signal [*1024,1034*] captured by the registered address input port; and

(d) defining a fourth route [*1058*] through said interconnect resources from a read clock sourcing circuit [*1053,54*] of the FPGA device to the at least one registered data output port.--

(Claim 20 is withdrawn.)

-- 20. 21. (Amended once) A method [*Fig. 11B*] for producing configuration signals for configuring an FPGA device having plural variable grain blocks (VGB's) [*102*], configurable interconnect resources, and an embedded memory subsystem comprising one or more memory blocks [*870*] situated for configurable coupling via the configurable interconnect resources to the VGB's, where the memory blocks each have at least one registered address input port [*872*] for receiving and storing supplied address bits in response to a supplied address-strobing signal [*933*] , and where the memory blocks each have at least one registered data output port [*882*] for storing and outputting retrieved read-data, the storing of the retrieved read-data being in response to a supplied data-strobing signal [*932*] , said method comprising the steps of:

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(a) inputting [*1106*] a design definition;

(b) searching [*1107*] the input design definition for the presence of one or more memory modules [*1110*], address-sourcing modules [*1120*], and data-using modules [*1170*] that will cooperate to perform a memory read or memory write operation; and

(c) encouraging [*1108*] the creation in the configured FPGA of a shared signal route [*1160,1060*] that transmits an address-strobing clock signal [*933,1015*] to the registered address input port and that transmits an address-change allowing signal [*1001*] to one or more of the address-sourcing modules [*1120,1023,1040*] and that transmits a data-strobing signal [*1059*] to one or more of the registered data output ports [*10R2,10R3*].--

--21 ~~22~~. (New) A field programmable gate array (FPGA) device [*1000*] comprising:

(a) a plurality of configurable logic blocks (CLB's) [*102, 1020*];

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(b) configurable CLB interconnect resources for configurably interconnecting said CLB's;

(c) a memory subsystem comprising:

(c.1) a plurality of independently-usable memory blocks [*470,480*] each having:

(c.1a) a shared array of memory cells [*901,902*];

(c.1b) a first port unit [*910*] coupled to the shared array and including a respective first data output port [*971*] and a first address input port [*918*];

(c.1c) a second port unit [*920*] coupled to the shared array and including a respective second data output port [*961*] and a second address input port [*928*], wherein the first and second port units can simultaneously access the shared array of memory cells;

(c.1d) first and second address-capturing registers [*911,921*] respectively coupled to the first and second address input ports, each address-capturing register having address and clock inputs and an address output;

(c.1e) first and second read-data capturing registers [*972,962*] respectively coupled to the first and second data output ports, each data capturing register having data and clock inputs and a data output;

(c.2) a configurable, first special interconnect channel [*1060*] that is programmably couplable [*1067-1069*] to said CLB interconnect resources,

(c.2a) said first special interconnect channel extending adjacent to a respective first group of said memory blocks;

(c.2b) said first special interconnect channel being further programmably couplable [*1065*] to the respective clock inputs of the first and second address-capturing registers of said first group of memory blocks such that the respective clock inputs of the first and second address-capturing registers of one or more memory blocks in the first group can be respectively driven by at least a first address-strobing signal [*1015*] which is transmitted by way of the first special interconnect channel; and

(c.2c) said first special interconnect channel being further programmably couplable [*1061,106D*] to the respective clock inputs of the first and second read-data capturing registers of said first group of memory blocks such that the respective clock inputs of the first and second read-data capturing registers of one or more memory blocks in the first group can be respectively driven by independent first and second data-strobing signals [*917,927*] which are transmitted by way of the first special interconnect channel.--

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-- 2283. (New) The FPGA device of Claim ~~22~~ wherein:

(c.2a1) said first special interconnect channel is programmably couplable [*1065*] to the respective clock inputs of the first and second address-capturing registers of said first group of memory blocks such that the clock input of the first address-capturing register of one or more memory blocks of the first group can be respectively driven by the first address-strobing signal [*1015*] and such that the clock input of the second address-capturing register of one or more memory blocks of the first group can be respectively driven by a second address-strobing signal [*1016*] which is independent of the first address-strobing signal [*1015*] and which is also transmitted by way of the first special interconnect channel.--

-- 23 24. (New) The FPGA device of Claim 21 22 wherein:

(c.2c) the configurable, first special interconnect channel [*1060*] is further programmably couplable [*1064,106C*] to the respective address inputs of the first and second address-capturing registers of said first group of memory blocks such that the respective address inputs of the first and second address capturing registers of one or more memory blocks of the first group can be respectively driven by independent first and second address signals [*ADR-SV1,ADR-SV2*] which are transmitted by way of the first special interconnect channel.--

-- 24 25. (New) The FPGA device of Claim 21 22 wherein:

(b.1) the configurable CLB interconnect resources include lines of diversified continuous lengths [*2xL-8xL,MaxL*] for configurably interconnecting said CLB's.--

-- 25 26. (New) The FPGA device of Claim 21 22 wherein:

(a.1) at least a plurality of said CLB's are constituted by variable grain blocks (VGB's) [*430*] where each said VGB is comprised of at least four Configurable Building Blocks (CBB's) and each CBB [*510*] can output to adjacent parts of the CLB interconnect resources at least one bit of processed result data, the processed result data bit being a configuration-defined function [*672*] of at least three input term signals that are acquirable by the CBB from adjacent parts of the CLB interconnect resources.--

-- 26 27. (New) The FPGA device of Claim 25 26 wherein:

(a.1a) each said processed result data bit of a given CBB can be programmably defined to be a configuration-defined function [*635*] of at least six input term signals that are acquirable by the CBB from adjacent parts of the CLB interconnect resources.--

-- 27. (New) The FPGA device of Claim 25 wherein:

(a.1a) each said processed result data bit of a given CBB can be programmably defined to be a configuration-defined function [*635/W0*] of at least sixteen input term signals that are obtainable from parts of the CLB interconnect resources that neighbor the given CLB.--

-- 28. (New) The FPGA device of Claim 25 wherein:

(a.1a) each said processed result data bit of a given CBB can be programmably defined to be a result [*638*] of an addition or subtraction operation [*570*] carried out at least partially within the given CBB.--

-- 29. (New) The FPGA device of Claim 25 wherein:

(b.1) said configurable CLB interconnect resources include continuous lines of diversified length including lines of a first continuous length [*2xL*] extending adjacent to at least two VGB's and lines of a second continuous length [*4xL,8xL*] extending adjacent to at least eight VGB's, the second continuous length being at least twice the first continuous length.--

-- 30. (New) The FPGA device of Claim 29 wherein:

(c.1c1) the second read-data capturing register [*962*] of each memory block is programmably couplable to at least an adjacent one of the first continuous length [*2xL*] lines.--

-- 31. (New) The FPGA device of Claim 30 wherein:

(c.1c2) the second port unit [*920*] of each memory block is a read-only port unit.--

-- 32. (New) The FPGA device of Claim 27 wherein:

(a.1a) said VGB's are disposed to define vertical columns of VGB's and horizontal rows of VGB's; and

(b.1) said configurable CLB interconnect resources include continuous lines of diversified length including lines of a first continuous length [*2xL*] extending adjacent to at least two VGB's and lines of a second continuous length [*MaxL*] extending adjacent to a respective full row or a full column of VGB's, the second continuous length being at least ten times the first continuous length.--

-- 33. (New) The FPGA device of Claim 32 wherein:

(c.1c1) the first and second read-data capturing registers [*962,972*] of each memory block are each programmably couplable to a respective at least one adjacent one of the second continuous length [*MaxL*] lines.--

-- 34. (New) The FPGA device of Claim 33 wherein:

(c.1c2) the second port unit [*920*] of each memory block is a read-only port unit while the first port unit [*910*] of each memory block is a read-write port unit.--

-- 35 36. (New) The FPGA device of Claim 21 22 wherein:

(c.1b1) said first port unit [*910*] includes a respective first data input port [*977*] for receiving write data for writing into said shared array of memory cells;

(c.1f) each given one of said memory blocks further includes a respective first write-data capturing register [*976,10R1*] respectively coupled to the first data input port [*977*] of the given memory block, each write-data capturing register having data and clock inputs and a data output;

(c.1f1) the respective clock input of each write-data capturing register in a given one of said memory blocks can be respectively driven by the corresponding first data-strobing signal [*917*] of the given memory block.--

-- 36 37. (New) The FPGA device of Claim 21 22 wherein:

(c.2c) said first special interconnect channel includes a plurality of continuous conductors of respectively diversified lengths [*S4xL,SMaxL*] including maximum length conductors [*862a*] for broadcasting to the first group of memory blocks common address bits, and including shorter length conductors [*864a*] for conveying other address bits to respective subsets the first group of memory blocks.--

-- 37 38. (New) The FPGA device of Claim 21 22 wherein:

(c.2c) said first special interconnect channel includes a plurality of continuous conductors of respectively diversified lengths [*S4xL,SMaxL*] including maximum length conductors [*862c*] for broadcasting to the first group of memory blocks common control bits, and including shorter length

conductors [*864c*] for conveying other control bits to respective subsets the first group of memory blocks.--

-- 39. (New) The FPGA device of Claim 38 wherein:

(c.2c1) said first special interconnect channel has global clock lines passing therethrough for broadcasting to the first group of memory blocks programmably acquirable global clock signals.--

-- 40. (New) The FPGA device of Claim 22 and further comprising:

(c.3) a configurable, second special interconnect channel [*166*] that is programmably couplable [*1067-1069*] to said CLB interconnect resources,

(c.3a) said second special interconnect channel extending adjacent to a respective second group [*116*] of said memory blocks;

(c.3b) said second special interconnect channel being further programmably couplable [*1065*] to the respective clock inputs of the first and second address-capturing registers of said second group of memory blocks such that the respective clock inputs of the first and second address-capturing registers of one or more memory blocks in the second group can be respectively driven by at least a second address-strobing signal [*1015*] which is transmitted by way of the second special interconnect channel; and

(c.3c) said second special interconnect channel being further programmably couplable [*1061,106D*] to the respective clock inputs of the first and second read-data capturing registers of said second group of memory blocks such that the respective clock inputs of the first and second read-data

capturing registers of one or more memory blocks in the second group can be respectively driven by independent third and fourth data-strobing signals [*917,927*] which are transmitted by way of the second special interconnect channel.--

-- 41. (New) A method of configuring a field programmable gate array (FPGA) device [*1000*] where the FPGA device comprises:

(0.1) a plurality of configurable logic blocks (CLB's) [*102, 1020*];

(0.2) configurable CLB interconnect resources for configurably interconnecting said CLB's;

(0.3) a memory subsystem comprising:

(0.31) a plurality of independently-usable memory blocks [*470,480*] each having:

(0.31a) a shared array of memory cells [*901,902*];

(0.31b) a first port unit [*910*] coupled to the shared array and including a respective first data output port [*971*] and a first address input port [*918*];

(0.31c) a second port unit [*920*] coupled to the shared array and including a respective second data output port [*961*] and a second address input port [*928*];

(0.31d) at least one address-capturing registers [*911,921*] respectively coupled to one of the first and second address input ports, the at least one address-capturing register having address and clock inputs and an address output;

(0.31e) at least one read-data capturing register [*972,962*] respectively coupled to one of the first and second data output ports, the at least one data capturing register having data and clock inputs and a data output;

(0.32) a configurable, special interconnect channel [*1060*] that is programmably couplable [*1067-1069*] to said CLB interconnect resources,

(0.32a) said special interconnect channel extending adjacent to said memory blocks;

(0.32b) said special interconnect channel being further programmably couplable [*1065*] to the respective clock inputs of the at least one address-capturing registers of said memory blocks such that the respective clock inputs of the at least one address-capturing registers of one or more of the memory blocks can be respectively driven by at least a first address-strobing signal [*1015*] which is transmittable by way of the special interconnect channel; and

(0.32c) said special interconnect channel being further programmably couplable [*1061,106D*] to the respective clock inputs of the at least one read-data capturing registers of said memory blocks such that the respective clock inputs of the at least one read-data capturing registers of one or more of the memory blocks can be respectively driven by a data-strobing signals [*917,927*] which is transmittable by way of the special interconnect channel;

said FPGA configuring method comprising:

(a) configuring [*1065*] the special interconnect channel to supply an address-strobing signal [*1015,ADRCLK1*] to the clock input of an address-capturing register of a given one of said memory blocks; and

(b) configuring [*1061*] the special interconnect channel to supply a data-strobing signal [*RWCLK1*] to the clock input of a read-data capturing register [*10R2*] of the given one

of said memory blocks such that the supplied address-strobing and data-strobing signals can be independent of one another.--

-- 41 42. (New) The FPGA configuring method of Claim 40 41 and further comprising:

(c) configuring [*1064*] the special interconnect channel to supply an address signal [*1019*] to the data input of an address-capturing register of the given one of said memory blocks.--

-- 42 43. (New) The FPGA configuring method of Claim 41 42 and further comprising:

(d) configuring [*1063*] a given one of said CLB's [*1023*] to be responsive to the supplied address-strobing signal and to produce a next and later address signal [*1027*] for the given memory block after said supplied address-strobing signal causes the address-capturing register of the given memory block to capture the earlier-supplied address signal [*1019*].--

-- 43 44. (New) The FPGA configuring method of Claim 41 42 and further comprising:

(d) configuring a given one of said CLB's [*1071,10D1*] to be responsive to the supplied data-strobing signal [*RWCLK3,1002*] and to produce an output enabling signal [*1072a,OE1*] that enables memory data to be output onto said CLB interconnect [*1075*] after the supplied data-strobing signal causes a read-data capturing register [*10R2*] of the given one of said memory blocks to capture resource memory read data.--

-- 44 ~~45.~~ (New) A field programmable gate array (FPGA) device [*1000*] comprising:

(a) a plurality of configurable logic blocks (CLB's) [*102, 1020*];

(b) configurable CLB interconnect resources for configurably interconnecting said CLB's;

(c) a memory subsystem comprising:

(c.1) a plurality of independently-usable memory blocks [*470,480*] each having:

(c.1a) a shared array of memory cells [*901,902*];

(c.1b) a first port unit [*910*] coupled to the shared array and including a respective first data output port [*971*] and a first address input port [*918*];

(c.1c) a second port unit [*920*] coupled to the shared array and including a respective second data output port [*961*] and a second address input port [*928*], wherein the first and second port units can access respectively addressed parts of the shared array of memory cells;

(c.1d) first and second address-capturing registers [*911,921*] respectively coupled to the first and second address input ports, each address-capturing register having address and clock inputs and an address output;

(c.1e) first and second read-data capturing registers [*972,962*] respectively coupled to the first and second data output ports, each data capturing register having data and clock inputs and a data output;

(c.2) a configurable, first special interconnect channel [*1060*] that is programmably couplable [*1067-1069*] to said CLB interconnect resources,

(c.2a) said first special interconnect channel extending adjacent to a respective first group of said memory blocks;

(c.2b) said first special interconnect channel being further programmably couplable [*1065*] to the respective clock inputs of the first and second

address-capturing registers of said first group of memory blocks such that the respective clock inputs of the first and second address-capturing registers of one or more memory blocks in the first group can be respectively driven by at least a first address-strobing signal [*1015,1057*] which is transmitted by way of the first special interconnect channel; and

(c.2c) said first special interconnect channel being further programmably couplable [*1061,106D*] to the respective clock inputs of the first and second read-data capturing registers of said first group of memory blocks such that the respective clock inputs of the first and second read-data capturing registers of one or more memory blocks in the first group can be respectively driven by one or more data-strobing signals [*1058,1059*] which are independent of the first address-strobing signal [*1057*] thereby allowing read-data-capture and address-capture operations by respective ones of the read-data capturing registers and address-capturing registers to occur at different times, and wherein said one or more data-strobing signals are transmitted [*1061,106D*] by way of the first special interconnect channel.--

-- 45 ~~46.~~ (New) The FPGA device of Claim ~~45~~ 44 wherein:

(c.2b1) the first special interconnect channel is programmably couplable [*1065,1066*] to the respective clock inputs of the first and second address-capturing registers of said first group of memory blocks such that the clock input of the first address-capturing register [*1011*] of one or more memory blocks of the first group can be respectively driven by the first address-strobing signal [*1015*] and such that the clock input of the second

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address-capturing register [*1012*] of one or more memory blocks of the first group can be respectively driven by a second address-strobing signal [*1016*] which is independent of the first address-strobing signal [*1015*] and which is also transmitted by way of the first special interconnect channel.--

-- 47. (New) The FPGA device of Claim 45 wherein:

(c.2d) the configurable, first special interconnect channel [*1060*] is further programmably couplable [*1064,106C*] to the respective address inputs of the first and second address-capturing registers of said first group of memory blocks such that the respective address inputs of the first and second address capturing registers [*1011,1012*] of one or more memory blocks of the first group can be respectively driven by independent first and second address signals [*ADR-SV1,ADR-SV2*] which are transmitted by way of the first special interconnect channel.--

-- 48. (New) The FPGA device of Claim 45 wherein:

(b.1) the configurable CLB interconnect resources include lines of diversified continuous lengths [*2xL-8xL,MaxL*] for configurably interconnecting said CLB's; and

(c.2d) the configurable, first special interconnect channel [*1060*] is programmably couplable to at least two different length conductors [*1051,1052*] of said CLB interconnect resources.--

-- 49. (New) The FPGA device of Claim 45 wherein:

(a.1) at least a plurality of said CLB's are constituted by variable grain blocks (VGB's) [*430*] where each said VGB is comprised of at least four Configurable Building Blocks (CBB's) and each CBB [*510*] can output to adjacent parts of the CLB interconnect resources at least one bit of processed result data, the processed result data bit being a configuration-defined function [*672*] of at least three input term signals that are acquirable by the CBB from adjacent parts of the CLB interconnect resources.--

-- ~~50~~ 49. (New) The FPGA device of Claim ~~49~~ 48 wherein:

(a.1a) each said processed result data bit of a given CBB can be programmably defined to be a configuration-defined function [*635*] of at least six input term signals that are acquirable by the CBB from adjacent parts of the CLB interconnect resources.--

-- ~~51~~ 50. (New) The FPGA device of Claim ~~49~~ 48 wherein:

(a.1a) each said processed result data bit of a given CBB can be programmably defined to be a configuration-defined function [*635/WO*] of at least sixteen input term signals that are obtainable from parts of the CLB interconnect resources that neighbor the given CLB.--

-- ~~52~~ 51. (New) The FPGA device of Claim ~~49~~ 48 wherein:

(a.1a) each said processed result data bit of a given CBB can be programmably defined to be a result [*638*] of an addition or subtraction operation [*570*] carried out at least partially within the given CBB.--

-- ~~53~~ 52. (New) The FPGA device of Claim ~~49~~ 48 wherein:

(b.1) said configurable CLB interconnect resources include continuous lines of diversified length including lines of a first continuous length [*2xL*] extending adjacent to at least two VGB's and lines of a second continuous length [*4xL,8xL*] extending adjacent to at least eight VGB's, the second continuous length being at least twice the first continuous length; and

(c.2d) the configurable, first special interconnect channel [*1060*] is programmably couplable to at least two different length conductors [*1051,1052*] of said CLB interconnect resources.--

-- ~~54.~~ 53 (New) The FPGA device of Claim ~~53~~ 52 wherein:

(c.1c1) the second read-data capturing register [*962*] of each memory block is programmably couplable to at least an adjacent one of the first continuous length [*2xL*] lines.--

-- ~~55.~~ 54 (New) The FPGA device of Claim ~~45~~ 44 wherein:

(c.1c1) the second port unit [*920*] of each memory block is a read-only port unit.--

-- ~~56.~~ 55 (New) The FPGA device of Claim ~~49~~ 48 wherein:

(a.1a) said VGB's are disposed to define vertical columns of VGB's and horizontal rows of VGB's; and

(b.1) said configurable CLB interconnect resources include continuous lines of diversified length including lines of a first continuous length [*2xL*] extending adjacent to at least two VGB's and lines of a second continuous length [*MaxL*] extending adjacent to a respective full row or a full column of VGB's, the second continuous length being at least ten times the first continuous length.--

-- 56 (New) The FPGA device of Claim 55 wherein:

(c.1c1) the first and second read-data capturing registers [*962,972*] of each memory block are each programmably couplable to a respective at least one adjacent one of the second continuous length [*MaxL*] lines.--

-- 57 (New) The FPGA device of Claim 56 wherein:

(c.1c2) the second port unit [*920*] of each memory block is a read-only port unit while the first port unit [*910*] of each memory block is a read-write port unit.--

-- 58 (New) The FPGA device of Claim 44 wherein:

(c.1b1) said first port unit [*910*] includes a respective first data input port [*977*] for receiving write data for writing into a portion of said shared array of memory cells that is addressed by the first address input port;

(c.1f) each given one of said memory blocks further includes a respective first write-data capturing register [*976,10R1*] respectively coupled to the first data input port [*977*] of the given memory block, each write-data capturing register having data and clock inputs and a data output;

(c.1f1) the respective clock input of each write-data capturing register in a given one of said memory blocks can be respectively driven by the corresponding first data-strobing signal [*917,RWCLK*] of the given memory block.--

-- 59 (New) The FPGA device of Claim 44 wherein:

(c.2d) said first special interconnect channel includes a plurality of continuous conductors of respectively diversified lengths [*S4xL,SMaxL*] including maximum length conductors [*862a*] for broadcasting to the first group of

memory blocks common address bits, and including shorter length conductors [*864a*] for conveying other address bits to respective subsets the first group of memory blocks.--

-- 61. (New) The FPGA device of Claim 45 wherein:

(c.2d) said first special interconnect channel includes a plurality of continuous conductors of respectively diversified lengths [*S4xL,SMaxL*] including maximum length conductors [*862c*] for broadcasting to the first group of memory blocks common control bits, and including shorter length conductors [*864c*] for conveying other control bits to respective subsets the first group of memory blocks.--

-- 62. (New) The FPGA device of Claim 61 wherein:

(c.2d1) said first special interconnect channel has global clock lines passing therethrough for broadcasting to the first group of memory blocks programmably acquirable global clock signals, where the global clock signals are also programmably acquirable by said CLB's for synchronizing operations of the CLB's.--

-- 63. (New) The FPGA device of Claim 45 and further comprising:

(c.3) a configurable, second special interconnect channel [*166*] that is programmably couplable [*1067-1069*] to said CLB interconnect resources,

(c.3a) said second special interconnect channel extending adjacent to a respective second group [*116*] of said memory blocks;

(c.3b) said second special interconnect channel being further programmably couplable [*1065*] to the respective clock inputs of the first and second address-capturing registers of said second group of memory blocks such that the respective clock inputs of the first and second address-capturing registers of one or more memory blocks in the second group can be respectively driven by at least a second address-strobing signal [*1015*] which is transmitted by way of the second special interconnect channel; and

(c.3c) said second special interconnect channel being further programmably couplable [*1061,106D*] to the respective clock inputs of the first and second read-data capturing registers of said second group of memory blocks such that the respective clock inputs of the first and second read-data capturing registers of one or more memory blocks in the second group can be respectively driven by independent third and fourth data-strobing signals [*917,927*] which are transmitted by way of the second special interconnect channel;

(c.3d) wherein said first and second special interconnect channels can programmably acquire same or different control signals from the CLB interconnect resources.--

-- 63 64. (New) The FPGA device of Claim 44 ~~45~~ wherein:

(a.1) each of said plurality of CLB's [*1020*] is programmably couplable to the first special interconnect channel by way of at least one tristateable line driver [*1031,1032*] such that different address signals [*1041,1042*] can be injected in time multiplexed fashion from

the CLB's to the first special interconnect channel by enabling outputs of different tristateable line drivers at different times; and

(a.2) output enable terminals [*1035,1036*] of said tristateable line drivers can be programmably made responsive [*1040*] to said at least first address-strobing signal [*1015,1043*] such that injection of a new and replacing address signal [*1027*] into the first special interconnect channel can be blocked until a previous address signal has been captured by a corresponding one of the address-capturing registers in response to said at least first address-strobing signal [*1043*].--

-- ~~65~~ 64 (New) The FPGA device of Claim ~~45~~ 44 wherein:

(c.1f) the data output ports of said first and second read-data capturing registers [*972,962*] can respectively couple [*884,882*] to the CLB interconnect resources by way of first and second tristateable line drivers [*974,964*], where each tristateable line driver has a respective output enable terminal [*943,944*];

(c.1g) the output enable terminals [*OE1,OE2*] of said tristateable line drivers can be programmably made responsive [*10D1,10D2*] to said one or more data-strobing signals [*ROCLK3"*] such that injection of new and replacing data signals [*10A2*] through the tristateable line drivers and into corresponding parts [*1075*] of the CLB interconnect resources can be blocked until said replacing data signals have been captured by corresponding ones of the data-capturing registers in response to said one or more data-strobing signals.--

-- ~~66~~ 65 (New) The FPGA device of Claim ~~45~~ 44 and further comprising:

(d) a plurality of programmably configurable input/output blocks (IOB's) [*700*] coupled to the CLB interconnect resources and having configurable I/O storage means